REMARKS

This Amendment is in response to the Office Action dated October 13, 2006.

Claims 7-20 and 23 have been rejected under 35 U.S.C. §112, second paragraph for allegedly not claiming the "the essential structural cooperative relationship(s) between" the claimed logic that maps, the logic that selectively enables' the logic that determines, the logic that advances, the logic that sets, the logic that dynamically modifies, and the logic that defines. The Office Action refers the Applicants to section 2172.01 of the MPEP.

MPEP §2172.01 entitled, "Unclaimed Essential Matter", discusses claims which omit matter disclosed to be essential to the invention as described in the specification or in other statements of record. However, the Office Action does not indicate portions of the specification or other statements in the record where the Applicants specifically state that the structural connections are necessary to practice the claimed invention, or define interrelationships between essential elements of the invention.

Applicants' description of Figures 3 and 4 (see page 5, paragraphs [0016] and [0017], page 6, paragraph [0022], and page 8, paragraph [0027] of Applicants' specification) refer to a system and method for interrupt mapping according to an aspect of the invention. The phrase "according to an aspect of the invention" indicates that the illustrations provided in the figures are exemplary, and that one of skill in the art may be able to derive a circuit or flow diagram, different from those illustrated in the figures, that comprise the claimed logic and method steps. Therefore, Applicants respectfully submit that specific structural connections, beyond

those recited in the present claims, are not necessary to point out the subject matter that applicants regard as their invention.

Based on the above, the Applicants assert that the claims comply with the requirements of 35 U.S.C. §112, and request withdrawal of the rejection of claims 7-20 and 23 under this section of the statute.

Page 4 of the Office Actions indicates that claims 22 and 23 have been rejected under 35 U.S.C. §112, second paragraph because the term "the same interrupt source" lacks antecedent basis. Applicants believe that the examiner meant to refer to claim 21, rather than 22, since this latter claim does not contain the indicated phrase. This rejection is addressed by the current amendment to claims 21 and 23. Therefore, the rejection of the claims on this ground should be withdrawn.

Claims 1, 7, 21 and 23 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,764,996 to Armstrong. Claims 1-23 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,530,875 to Wach.

The Armstrong patent is directed to a method and apparatus that is intended to overcome a limitation in the shared interrupt scheme of the PCI Local Bus Specification, Revision 2.1, in which the host CPU is required to interrogate PCI devices, a so-called "Polling Method," after receiving an interrupt request in order to determine which PCI device initiated that interrupt. (see column 1, lines 41-46).

Applicants' claims are also directed to an apparatus and method that overcomes the polling methods of the prior art (see Applicants' specification at page

2, paragraph [0006]). Therefore, Applicants' respectfully submit that they are not attempting to claim the PCI Local Bus Specification as allegedly by the Examiner on page 5 of the Office Action.

The Office Action cites column 1, lines 37-43, column 2, lines 56-67, and Figure 2 of the Armstrong patent as disclosing the claimed features. However, column 1, lines 37-43 merely describes the above-mentioned PCI Local Bus Specification. While Applicants appreciate the inclusion of figures from the applied art in the Office Action, neither the figures, the cited text nor the discussion in the Office Action discloses the claimed logic that maps each of the plurality of interrupt sources to each of the plurality of interrupt inputs.

Since the claimed interrupt sources of the reference have not been identified in the Office Action, Applicants assume that INTA, INTB, INTC and INTD of each PCI device, 18, 20, 22 and 24 of the Armstrong patent, are being interpreted as the interrupt sources. In addition, the Applicants understand the Office Action to be interpreting INTA 52, INTB 54, INTC 56 and INTD 58 as the interrupt inputs. The description of Figure 2 of the Armstrong patent does not indicate that each INTA, INTB, INTC and INTD of each PCI device 18, 20, 22 and 24 is mapped to each interrupt input. For instance, there is no disclosure that INTA of PCI device 18 is mapped to INTB 54, INTC 56 and INTD 58. Applicants respectfully submit that each of the plurality of interrupt sources is not mapped to each of the plurality of interrupt inputs, as recited in the independent claims. Rather, each interrupt source is only mapped to one interrupt input. As such, the Armstrong patent is representative of the prior art illustrated in Figure 1 of the present application.

Applicants respectfully disagree with the Examiner's characterization that in all cases a logic OR gate can be used to "selectively" enable an input that is being asserted. The word "selectively" means discriminating of or characterized by selection. (see American Heritage College dictionary, 1235 (Robert B. Costello ed., 3rd Edition, Houghton Mifflin Co. 2000). In the Armstrong patent, by merely being asserted, INTA of PCI device 18 will cause INTA 52 to also be a asserted. There is no discrimination in the operation of an OR gate. As shown in the table on page 7 of the Office Action, if an interrupt is present at the input to the gate (represented by the logic "1"), it gets passed along to the output of the gate. There is no selectivity whatsoever in the Armstrong patent, merely the pass-through operation of a logic OR gate.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that the Armstrong patent does not expressly or inherently describe each and every element of claims 1, 7, 21 and 23. Therefore, the rejection of claims1, 7, 21 and 23 over the Armstrong patent should be withdrawn.

Claims 1-23 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,530,875 to Wach.

The Wach patent describes a processor-based architecture (see Abstract of the Wach patent) that has a limited number of interrupt inputs. The Wach patent specifically describes a disk drive controller 10 that is a processor-based electronic

device coupled to the standard small computer standard interface (SCSI) (See column 3, lines 60-65). In the embodiment shown in Fig. 1, the controller has three interrupt inputs, 26, 28 and 30.

Applicants' independent claims substantially recite the feature of mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs. The Office Action at page 9, line 3 states that the claimed plurality of interrupt inputs are represented by the plurality of storage locations GF described in the Wach patent. Applicants respectfully traverse this assertion.

As disclosed in the Wach patent, the storage locations GF are part of group register 44, which must be read by the processor 14. The Wach patent refers to the storage locations GF as interrupt groups. Basically, each successive pair of interrupt sources forms an interrupt group (see column 6, lines 9-21). The register 44 is associated with one of the interrupt inputs, namely interrupt line 26. When an interrupt is received on this line, the register 44 identifies which group contains the interrupt source that generated the interrupt (column 6, lines 21-24).

The operation of the system described in the Wach patent is different from the operation of the claimed method and apparatus. In the Wach patent, the register 44 must be read by the processor 14 in order for the interrupt source to be identified (column 6, lines 21-24 of the Wach patent). This is one of the drawbacks of the prior art identified in Applicants' specification (see paragraph [0006] of Applicants' specification). It is a drawback because the interrupt manager 38 and processor 14 must determine which interrupt source is issuing the interrupt request by polling the

interrupt group in register 44. The Wach patent merely reduces the number of times the processor polls the register as described at column 6, lines 25-35.

Applicants respectfully submit that the claimed interrupt inputs are not the same as the plurality of locations GF of register 44 disclosed in the Wach patent. The plurality of locations GF are merely storage locations read by the processor 14 in response to an interrupt request on line 26.

Applicants' respectfully submit that the Wach patent does not disclose or suggest all of the features recited in Applicants' independent claims, in particular, the feature of mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs, or logic that maps each of the plurality of interrupt sources to each of the plurality of interrupt inputs.

The rejections of claims 1-23 over the Wach patent should be withdrawn for at least the above reasons.

Should any questions arise in connection with this application, or should the Examiner believe a telephone conference would be helpful in resolving any remaining issues pertaining to this application, the undersigned respectfully requests that he be contacted at the number indicated below.

Respectfully submitted,
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